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List of published papers in national/ international conference proceedings during the year 2017

S. No.	Title of the Conference Paper	Page No.
1.	Advanced seven level transformer-less multilevel inverter topology for PV application	1-2
2.	Architecture based performance evaluation of IIR digital filter for DSP applications	3-4
3.	Design and implementation of efficient IIR LMS adaptive filter with improved performance	5-6
4.	Hand written symbol recognition using hierarchical shape representation model based on shape signature	7-10
5.	Novel Hash Based Key Generation for Stream Cipher in Cloud	11-14



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Advanced seven level transformer-less multilevel inverter topology for PV application

Publisher: IEEE

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N. Rajanand Patnaik ; Y. Ravindranath Tagore ; S. Chaitanya All Authors

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Maximum Power Point Tracker (MPPT) for Photovoltaic Power Systems-A Systematic Literature Review

2018 European Control Conference (ECC)
Published: 2018

Evaluation of the "Hill Climbing" and the "Incremental Conductance" Maximum Power Point Trackers for Photovoltaic Power Systems

IEEE Transactions on Energy Conversion
Published: 2012

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Abstract



Document Sections

- I. Introduction
- II. Design of PV Power System
- III. Simulation Analysis
- IV. Conclusion

Abstract:In the present trend the Renewable Energy Sources (RES) are the main alternative concept to develop the power generation and it is cheap compared to other sources. The RE... [View more](#)

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Abstract:

In the present trend the Renewable Energy Sources (RES) are the main alternative concept to develop the power generation and it is cheap compared to other sources. The RES (Renewable Energy Sources) like solar energy, wind energy, geothermal energy, biomass, tidal power etc., and here among all these sources of energy solar module is developed with two individual boosts converters are utilized to step-up the voltage with Maximum Power Point P&O (Perturb & Observe) technique. The fundamental concentration of this paper is to present the advanced multilevel competitive inverter topology with reduction in device count is the main merit of this topology which is called Packed U Cell (PUC). The main issue of previously designed multilevel inverter topologies is bulk in complex structures; hence it affects the overall system in terms of cost. Due to the excellent characteristics of Packed U Cell topology there is no need of filter requirement, because of output voltage and current are nearer to sinusoidal. To highlight the merits and performance of this proposed concept was simulating in MATLAB/Simulink.

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Published in: 2017 Third International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)

Date of Conference: 27-28 February 2017
INSPEC Accession Number: 17040069

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ISBN:978-1-5090-5434-3

Print on Demand(PoD)

ISBN:978-1-5090-5435-0

Conference Location: Chennai, India

N. Rajanand Patnaik
Department of EEE, VLITS, Guntur, India

Y. Ravindranath Tagore
Department of EEE, VLITS, Guntur, India

S. Chaitanya
Department of EEE, AEC, Kakinada, India

☰ Contents

I. Introduction

In this modern trend of renewable energy sources, the demand for developing the PV system is increasing day by day because of excellent characteristics in main aspects compared to the other renewable sources. In present days PV installations are increasing exponentially mainly with support of government to develop the green energy concept. One of the foremost vital varieties of PV installation is that the grid connected electrical converter configurations. These grid connected PV systems is classified from two main points: PV cell and electrical converter configurations Fig. 1. The PV cell should be classified into five groups: string, multi-string, AC-cell, AC-module and centralized technology.

Authors ^

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Figures v

References v

Citations v

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Architecture based performance evaluation of IIR digital filters for DSP applications

Publisher: IEEE

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P. Bujjibabu; N. Sravani All Authors

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An innovative approach for RMS and THD control by field programmable gate arrays
The Fifth International Conference on Power Electronics and Drive Systems, 2003. PEDS 2003.
Published: 2003

FPGA implementation of Kalman low-pass filter for applications in sigma-delta (/spl Sigma/-/spl Delta/) demodulation
2003 IEEE Workshop on Signal Processing Systems (IEEE Cat. No.03TH8682)
Published: 2003

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Document Sections

- I. Introduction
- II. Digital Filters
- III. IIR Filter
- IV. Design and Implementation
- V. Implementation of a Filter
- Show Full Outline ▾

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Abstract: A relatively recent innovation in the domain of digital filtering has been the introduction of signal processing applications with effective power utilization. No scope t... [View more](#)

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Abstract:

A relatively recent innovation in the domain of digital filtering has been the introduction of signal processing applications with effective power utilization. No scope towards the effective and efficient architecture realization with existing part of literature, and hence investigation is made and is confined with cascade form of filter design. In this paper, architectures are realized based on common set of specifications to arrive at the high performance recursive filter for low power applications using Xilinx System Generator. Infinite Impulse Response (IIR) filters can be realized in many forms those are Direct form-I, Direct form-II, Cascade, parallel form. All these structures provide a space for selection of an appropriate architecture for reduction of power consumption and improvement in speed of digital filters. In this particular work, a 5th order low pass IIR filter is realized in Direct form-I, Direct form-II, Cascade form (Direct form-I/ Direct form-II) as an example of the methodology in a Xilinx FPGA device. Also corresponding power analysis was performed and finally concluded that cascade (Direct form-I) realization is the best technique to implement higher order IIR filters when power is a main constraint, cascade (Direct form-II) technique is best with area and speed as constraints.

Published in: 2017 International Conference on Big Data Analytics and Computational Intelligence (ICBDAC)

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2017

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17261528

Date Added to IEEE Xplore: 19
October 2017

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USB ISBN:978-1-5090-6399-4

Print on Demand(PoD)

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Conference Location: Chirala, Andhra
Pradesh, India

P. Bujjibabu

Aditya Engineering College, low power VLSI Design ()

N. Sravani

Department of ECE, Aditya Engineering College, Andhra Pradesh, India

☰ Contents

I. Introduction

NEED FOR LOW POWER: Reduction of power consumption and dissipation [11] [12] is significantly important for all high performance systems since it is desirable to maximize the run time with minimum requirements in size, battery life and weight of batteries. That's why the technology with low power consumption has become a major subject in today's electronic world.

Authors

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Design and implementation of efficient IIR LMS adaptive filter with improved performance

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Design and implementation of least mean square adaptive filter on Altera Cyclone II Field Programmable Gate Array for active noise control

2009 IEEE Symposium on Industrial Electronics & Applications

Published: 2009

The Implementation of a High Speed Adaptive FIR Filter on a Field Programmable Gate Array

MELECON 2006 - 2006 IEEE Mediterranean Electrotechnical Conference

Published: 2006

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Abstract



Document Sections

- I. Introduction
- II. Adaptive Filter
- III. LMS Filter Algorithm
- IV. Analysis of Existing and Proposed Designs
- » Conclusion

Abstract: The evolution of multi-feature portable devices with high speed processors and with drastic growth in component density turns the designer attention towards power aware d... [View more](#)

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Abstract:

The evolution of multi-feature portable devices with high speed processors and with drastic growth in component density turns the designer attention towards power aware design schemes. In low power VLSI designs an adaptive filter can obtain a reduction in terms of area and power consumption. A system with a linear transfer function controlled by variable parameters and a means to adjust those parameters according to an optimization algorithm is called adaptive filter. The Least Mean Square (LMS) filter is one of adaptive filters type which is used commonly, because of its simplicity and also because of its satisfactory convergence performance. The current IIR adaptive filter uses LMS to reduce area-delay product and energy-delay product. To reduce this delay one can implement filter in pipelined structure. Shift-add tree efficiently minimizes the critical path and silicon area without increasing the number of adaptation delays. The structure of IIR adaptive filter designing is done by using two main blocks: IIR block and new coefficients block (weights block). Weights block consists of series of partial product generators and shift/add tree. Partial product generators has 2 to 3 decoders and AND/OR cells. Weights block performs multiply accumulate operations. Filter block depends upon the new filter coefficients obtaining from weights block. The proposed filter is designed in MATLAB (2013a) for its performance characteristics and its constraints are verified using XILINX (ver14.7) implemented on FPGA.

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2/14
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ISBN:978-1-5090-6401-4

Conference Location: Chirala, Andhra Pradesh, India

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Aditya Engineering College, Low power VLSI Design

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☰ Contents

I. Introduction

DIGITAL filters are indispensable elements in signal processing and find numerous applications in industrial electronics like, power system, automatic control, and communications engineering. At the time of 1950s, they began to be interjecting in the literature. With the eloquence advancements in digital technologies, digital filters began to offer cognizant puritanical solutions to many problems of the past.

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References v

Citations v

Keywords v

Metrics v

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Proceedings of International Conference on Computational Intelligence and Data Engineering

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Editors: Nabendu Chaki, Agostino Cortesi, Nagaraju Devarakonda

Presents novel ideas in most-happening areas of computational intelligence and data engineering

Discusses a comprehensive understanding of the challenges of technological advancements from different viewpoints

Serves as a reference material for advance research

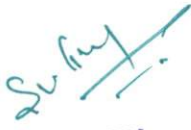
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Proceedings of International Conference on Computational Intelligence and Data Engineering pp 293–300

Handwritten Symbol Recognition Using Hierarchical Shape Representation Model Based on Shape Signature

M. Raja Babu , T. Gokaramaiah & A. Vishnuvardhan Reddy

Conference paper | First Online: 21 December 2017

512 Accesses

Part of the Lecture Notes on Data Engineering and Communications Technologies book series
(LNDECT, volume 9)

Abstract

The Signature represents visual object shape 2D contour in 1D to recognition shape of the objectQuery. This 1D shape representation translated into Centroid Distance Histogram (CDH) Gokaramaiah et al. (Comput Graph Image Process 25:357–370, 1974 [16]) to achieve invariant transformations such as translation, scale, rotation, flip. The CDH representation performs well in content-based image retrieval system with low computational complexity and this representation



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19. O. Starostenko, C. K. Cruz, A. Chavenz-Aragon, and R. Contreras. A novel shape indexing method for automatic classification of lepidoptera. *IEEE Computer Society*, 2007.
-

Author Declaration

We the undersigned declare that this manuscript is original, has not been published before and is not currently being considered for publication

elsewhere. We confirm that all ethical approvals have been granted to the authors regarding data managed in this research. We further confirm that any aspect of the work covered in this manuscript has been conducted with the ethical approval of all relevant bodies and that such approvals are acknowledged within the manuscript.

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Hierarchical Shape Representation Model Based on Shape Signature. In: Chaki, N., Cortesi, A., Devarakonda, N. (eds) Proceedings of International Conference on Computational Intelligence and Data Engineering. Lecture Notes on Data Engineering and Communications Technologies, vol 9. Springer, Singapore.
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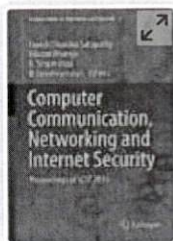
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Computer Communication, Networking and Internet Security

Proceedings of **IC3T 2016**

Editors: Suresh Chandra Satapathy, Vikrant Bhateja,
K. Srujan Raju, B. Janakiramaiah

Includes supplementary material: sn.pub/extras

Part of the book series: Lecture Notes in Networks and Systems (LNNS, volume 5)

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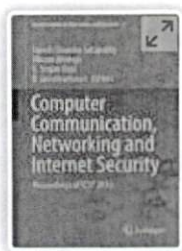
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Computer Communication, Networking and Internet Security pp 283–290

Novel Hash Based Key Generation for Stream Cipher in Cloud

K. DeviPriya  & L. Sumalatha

Conference paper | First Online: 04 May 2017

897 Accesses

Part of the Lecture Notes in Networks and Systems book series (LNNS, volume 5)

Abstract

Cloud Computing is an advanced technology which provides services to the users on rental basis. Cloud minimizes the installation cost of hardware, software, applications setup at client side and these services are available at cloud server, accessed by any one, any time, any place through the internet. Apart from the benefits one big challenge faced by the cloud is security problem as the data and resources are not under the control of data owner. Security techniques are required to protect data from the unauthorized access. In this paper, we proposed simple efficient stream cipher to protect information which is stored in the cloud. Also a hash based key is generated for encryption. The

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